REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. - lgt	02-04-18	Raymond Monnin
B	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	14-04-17	Charles Saffle

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Sandra Rooney

APPROVED BY
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DRAWING APPROVAL DATE
92-12-16

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, CMOS, 16-BIT, 20 KHZ, A/D CONVERTER, MONOLITHIC SILICON

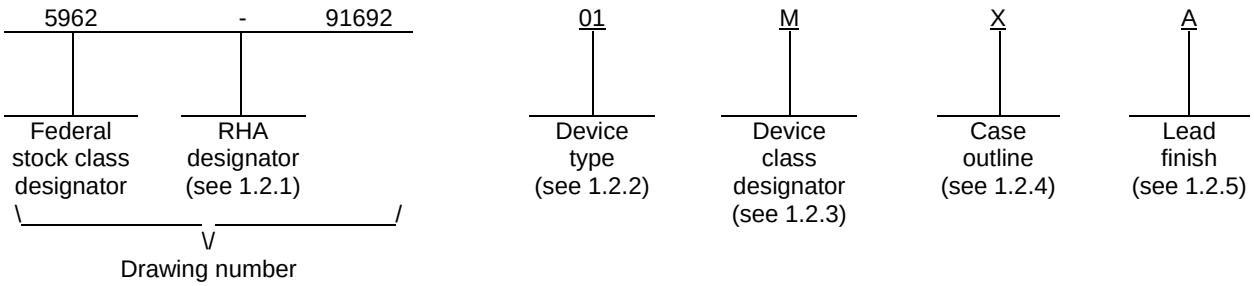
SIZE	CAGE CODE	
A	**67268**	**5962-91692**

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Linearity error
01	SEI5102A-S	16-bit, 20 kHz analog to digital converter	±3.0 LSB
02	SEI5102A-T	16-bit, 20 kHz analog to digital converter	±2.0 LSB

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/, 2/

Positive digital supply ($+V_D$) voltage range	-0.3 V dc to +6.0 V dc 3/
Negative digital supply ($-V_D$) voltage range	+0.3 V dc to -6.0 V dc
Positive analog supply ($+V_A$) voltage range	-0.3 V dc to +6.0 V dc
Negative analog supply ($-V_A$) voltage range	+0.3 V dc to -6.0 V dc
Input current, any pin except supplies	±10 mA 4/
Analog input voltage (AIN and VREF pins)	($-V_A$) – 0.3 V dc to ($+V_A$) + 0.3 V dc
Digital input voltage	-0.3 V dc to ($+V_A$) + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+160°C
Power dissipation (P_D)	72 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case J	40°C/W
Case 3	60°C/W

1.4 Recommended operating conditions. 1/

Ambient operating temperature range (T_A)	-55°C to +125°C
Positive digital supply voltage ($+V_D$)	+4.50 V dc to $+V_A$
Negative digital supply voltage ($-V_D$)	-4.50 V dc to -5.50 V dc
Positive analog supply voltage ($+V_A$)	+4.50 V dc to +5.50 V dc
Negative analog supply voltage ($-V_A$)	-4.50 V dc to -5.50 V dc
Analog reference voltage (VREF)	+2.50 V dc to ($+V_A$) -0.5 V dc
Analog input voltage range:	
Unipolar	AGND V dc to V_{REF}
Bipolar	$-V_{REF}$ to V_{REF}

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ All voltages referenced to AGND and DGND tied together.
2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ In addition, $+V_D$ must not be greater than ($+V_A$) + 0.3 V dc.
4/ Transient currents of up to 100 mA will not cause latch-up.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block or logic diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	1/ Limits		Unit
					Min	Max	
Resolution for which no missing codes is guaranteed	RES	2/	1, 2, 3	All	16		Bits
Integral linearity error	INL	2/	1, 2, 3	01		±3.0	LSB
				02		±2.0	
Full-scale error	FSE	2/	1, 2, 3	01		±5.0	LSB
				02		±3.0	
Full-scale error drift	ΔFSE/Δt	2/, 3/, 4/	2, 3	All		±4.0	LSB
Unipolar offset error	VOFF	2/	1, 2, 3	01		±5.0	LSB
				02		±3.0	
Unipolar offset error drift	ΔVOFF/Δt	2/, 3/, 4/	2, 3	All		±4.0	LSB
Bipolar offset error	BOFF	2/	1, 2, 3	01		±5.0	LSB
				02		±3.0	
Bipolar offset error drift	ΔBOFF/Δt	2/, 3/, 4/	2, 3	All		±4.0	LSB
Bipolar negative full-scale error	BNFSE	2/	1, 2, 3	01		±5.0	LSB
				02		±3.0	
Bipolar negative full-scale error drift	ΔBNFSE/Δt	2/, 3/, 4/	2, 3	All		±4.0	LSB
Digital input voltage	V_{IH}	5/, 6/, 7/	1, 2, 3	All	2.0		V
	V_{IL}					0.8	
Digital input current	I_{IN}	5/, 6/	1, 2, 3	All		±10	μA
Digital output voltage	V_{OL}	5/, 6/ Logic "0", I_{SINK} = -1.6 mA	1, 2, 3	All		0.4	V
	V_{OH}	5/, 6/ Logic "1", I_{SOURCE} = 100 μA			+VD -1.0		
Positive analog supply current	I_A+	2/, 6/, 8/ $+V_A$ = 5.5 V dc	1, 2, 3	All		3.5	mA
Negative analog supply current	I_A-	2/, 6/, 8/ $-V_A$ = -5.5 V dc	1, 2, 3	All		-3.5	mA
Positive digital supply current	I_D+	2/, 6/, 8/ $+V_D$ = 5.5 V dc	1, 2, 3	All		3.5	mA
Negative digital supply current	I_D-	2/, 6/, 8/ $-V_D$ = -5.5 V dc	1, 2, 3	All		-2.5	mA
Analog input capacitance in fine charge mode	C_{IN}	2/, 3/ Unipolar mode	4	All		425	pF
		2/, 3/ Bipolar mode				265	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	1/ Limits		Unit
					Min	Max	
Peak harmonic or spurious noise	S/PN	2/	4, 5, 6	01	94		dB
				02	98		
Signal to noise ratio	S/(N+D)	2/	4, 5, 6	01	87		dB
				02	90		
Acquisition time	t_{ACQ}	2/, 3/, 9/	9	All		9.375	µs
Conversion time	t_C	2/, 6/	9, 10, 11	All		40.63	µs
Throughput	f_{tp}	2/, 6/	9, 10, 11	All	20		kHz
$\overline{RST}$ pulse width	t_{RST}	3/, 5/, 10/ (see figure 3)	9, 10, 11	All	150		ns
CH1/$\overline{2}$ edge to $\overline{TRK1}$, $\overline{TRK2}$, falling	t_{DFSH4}	5/, 6/, 10/, 11/ (see figure 4a)	9, 10, 11	All		68 t_{clk} +260	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, falling	t_{DFSH1}	5/, 6/, 10/, 12/ (see figure 4b)	9, 10, 11	All	66 t_{clk}	68 t_{clk} +260	ns
$\overline{HOLD}$ pulse width	t_{HOLD}	5/, 6/, 10/, 12/ (see figure 5)	9, 10, 11	All	1 t_{clk} +20	63 t_{clk}	ns
$\overline{HOLD}$ to CH1/$\overline{2}$ edge	t_{DHLRI}	5/, 6/, 10/, 12/ (see figure 5)	9, 10, 11	All	15	64 t_{clk}	ns
$\overline{HOLD}$ falling to CLKIN falling	t_{HCF}	5/, 6/, 10/, 12/ (see figure 6)	9, 10, 11	All	95	1 t_{clk} +10	ns
SCLK input pulse period	t_{SCLK}	5/, 6/, 10/ (see figure 7a) PDT and RBT modes	9, 10, 11	All	200		ns
SCLK input pulse width low	t_{SCLKL}	5/, 6/, 10/ (see figure 7) PDT and RBT modes	9, 10, 11	All	50		ns
SCLK input pulse width high	t_{SCLKH}	5/, 6/, 10/ (see figure 7) PDT and RBT modes	9, 10, 11	All	50		ns
SCLK input falling to SDATA valid	t_{DSS}	5/, 6/, 10/ (see figures 7 and 8) PDT and RBT modes	9, 10, 11	All		150	ns
SDATA valid before rising SCLK	t_{SS}	5/, 6/, 10/ (see figure 8b) FRN and SSC modes	9, 10, 11	All	2 t_{clk} -100		ns
SDATA valid after rising SCLK	t_{SH}	5/, 6/, 10/ (see figure 7b) FRN and SSC modes	9, 10, 11	All	2 t_{clk} -100		ns
Last rising SCLK to SDL rising	t_{RSDL}	5/, 6/, 10/ (see figure 7b) FRN and SSC modes	9, 10, 11	All		2 t_{clk} +200	ns
$\overline{HOLD}$ falling to 1st falling SCLK	t_{HFS}	5/, 6/, 10/ (see figure 7b) FRN and SSC modes	9, 10, 11	All	6 t_{clk}	8 t_{clk} +200	ns
$\overline{HOLD}$ falling to SDATA valid	t_{DHS}	5/, 6/, 10/ (see figure 8a) PDT mode	9, 10, 11	All		230	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	1/ Limits		Unit
					Min	Max	
$\overline{TRK1}$, $\overline{TRK2}$ falling to SDATA valid	t_{DTS}	5/, 6/, 10/, 13/ (see figure 8b)	9, 10, 11	All		125	ns
CLKIN period	t_{CLK}	3/, 5/, 6/, 10/, 14/ (see figure 6)	9, 10, 11	All	0.5	10	μs
CLKIN low time	t_{CLKL}	5/, 6/, 10/ (see figure 6)	9, 10, 11	All	200		ns
CLKIN high time	t_{CLKH}	5/, 6/, 10/ (see figure 6)	9, 10, 11	All	200		ns

1/ The limiting terms “min” (minimum) and “max” (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

2/ Unless otherwise specified, $+V_A$, $+V_D$ = +5.0 V dc; $-V_A$, $-V_D$ = -5.0 V dc; VREF = +4.5 V dc; CLKIN = 1.6 MHz; f_s = 20 kHz; bipolar mode; FRN mode; AIN1 and AIN2 tied together; each channel tested separately; analog source impedance = 50Ω with 1000 pF to AGND; 200 Hz full scale input sine wave; error tests are done after calibration at the temperature of interest; logic “0” inputs are 0 V dc; logic “1” inputs are $+V_D$.

3/ This parameter shall be measured only for initial characterization and after process or design changes which may affect this parameter.

4/ Total drift over -55°C to +125°C since calibration at power-up at +25°C.

5/ $+V_A$, $+V_D$ = +5.0 V dc ±10 percent; $-V_A$, $-V_D$ = -5.0 V dc ±10 percent.

6/ This parameter is guaranteed, if not tested, at T_A = +25°C. This parameter is tested at T_A = -55°C to +125°C.

7/ Guaranteed at V_{IH} = 2.0 V dc, V_{IL} = 0.8 V dc. Tested at $V_{IH} = +V_D$, V_{IL} = 0 V dc.

8/ All outputs unloaded; inputs: Logic “0” = 0 V dc, Logic “1” = $+V_D$.

9/ Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.

10/ Inputs: Logic “0” = 0 V dc, Logic “1” = $+V_D$; C_L = 50 pF.

11/ These times are for FRN mode.

12/ These times are for SSC, PDT and RBT mode.

13/ Only valid for $\overline{TRK1}$, $\overline{TRK2}$ falling when SCLK is low. If SCLK is high when $\overline{TRK1}$, $\overline{TRK2}$ falls, then SDATA is valid t_{DSS} time after the next falling clock.

14/ Clock speeds of less than 1.6 MHz, at temperatures > +100°C, will degrade DNL performance. Minimum CLKIN period is 0.625 μs in FRN mode (20 kHz sample rate).

Device types	01 and 02
Case outlines	X, 3
Terminal number	Terminal symbol
1	$-V_D$
2	$\overline{RST}$
3	CLKIN
4	XOUT
5	$\overline{STBY}$
6	DGND
7	$+V_D$
8	$\overline{TRK1}$
9	$\overline{TRK2}$
10	CRS/ $\overline{FIN}$
11	SSH/SDL
12	$\overline{HOLD}$
13	CH1/ $\overline{2}$
14	SCLK
15	SDATA
16	CODE
17	BP/ $\overline{UP}$
18	OUTMOD
19	AIN1
20	V_{REF}
21	REFBUF
22	AGND
23	$-V_A$
24	AIN2
25	$+V_A$
26	$\overline{TEST}$
27	SCKMOD
28	$\overline{SLEEP}$

FIGURE 1. Terminal connections.

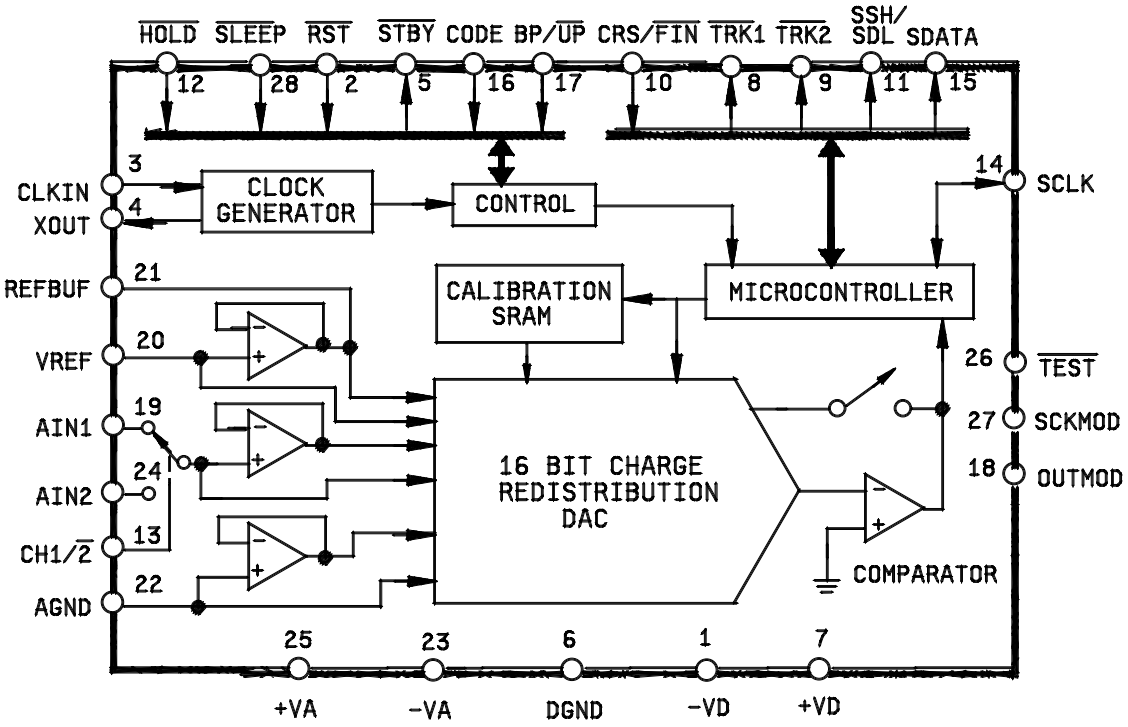


FIGURE 2. Block diagram.

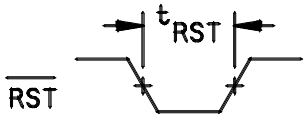


FIGURE 3. Reset timing.

NOTE: All measurements taken at 50 percent of the rise and fall edges.

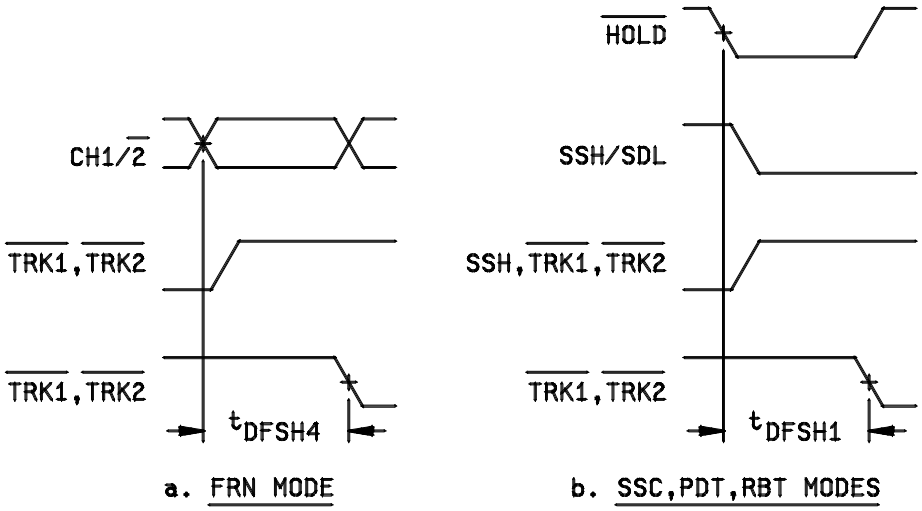


FIGURE 4. Control output timing.

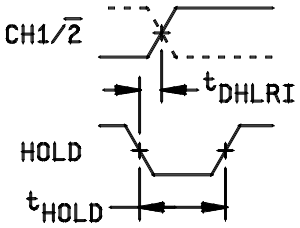


FIGURE 5. Channel selection timing.

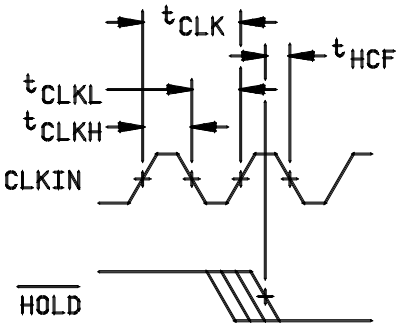


FIGURE 6. Start conversion timing.

NOTE: All measurements taken at 50 percent of the rise and fall edges.

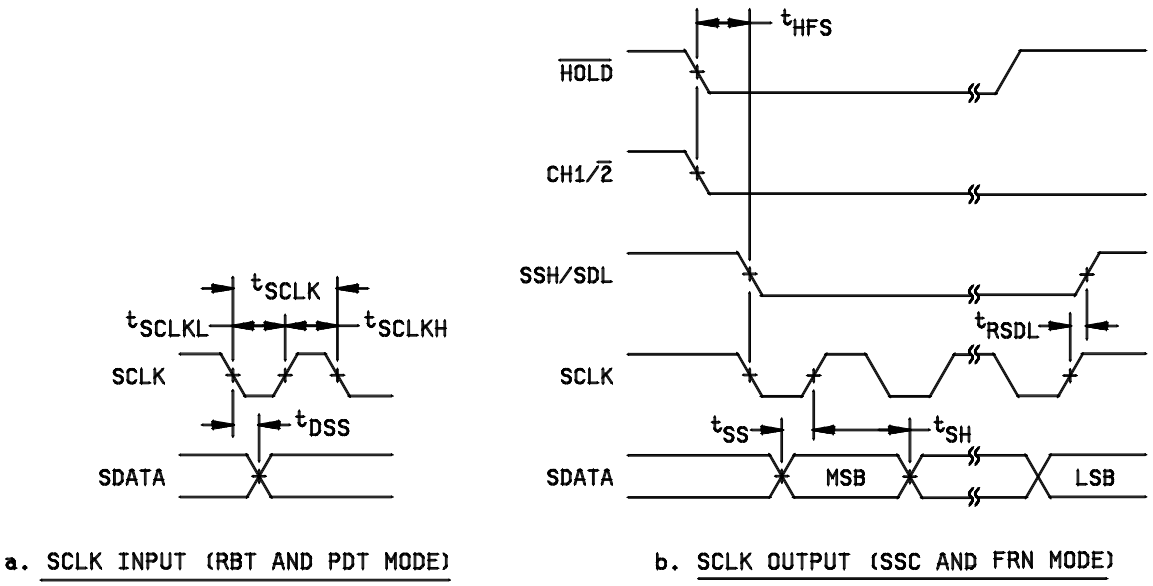


FIGURE 7. Serial data timing.

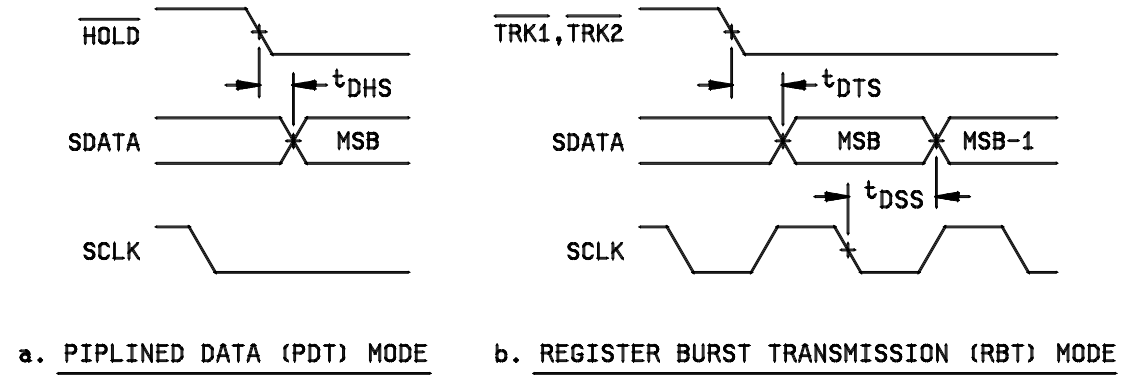


FIGURE 8. Data transmission timing.

NOTE: All measurements taken at 50 percent of the rise and fall edges.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4	1, 4	1, 4
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 10, 11 1/	1, 2, 3, 4, 5, 6, 10, 11 1/	1, 2, 3, 4, 5, 6, 10, 11 1/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11 2/	1, 2, 3, 4, 5, 6, 9, 10, 11 2/	1, 2, 3, 4, 5, 6, 9, 10, 11 2/
Group C end-point electrical parameters (see 4.4)	1, 4, 9	1, 4, 9	1, 2, 3, 4, 5, 6, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 4, 9	1, 4, 9	1, 4, 9
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.
2/ Subgroup 9 will be guaranteed if not tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-04-17

Approved sources of supply for SMD 5962-91692 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9169201M3A	68911	SEI5102A-SEB
5962-9169201Q3C	68911	SEI5102A-SEB
	3RNH0	5102A-SEB
5962-9169201MXA	68911	SEI5102A-SDB
5962-9169201QXC	68911	SEI5102A-SDB
	3RNH0	5102A-SDB
5962-9169202M3A	68911	SEI5102A-TEB
5962-9169202Q3C	68911	SEI5102A-TEB
	3RNH0	5102A-TEB
5962-9169202MXA	68911	SEI5102A-TDB
5962-9169202QXC	68911	SEI5102A-TDB
	3RNH0	5102A-TDB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
68911	Maxwell Technologies Electronics Components Group, Inc. 9244 Balboa Ave. San Diego, CA 92123
3RNH0	XTREME Semiconductor 2801 Oakmont Drive, Bldg. A, Suite 700 Round Rock, TX 78664